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Single phase seven level Z-source cascaded H-bridge inverter for photovoltaic systems

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ABSTRACT

The Multilevel inverter (MLI) is identified as a viable power electronic unit for distributed energy conversion applications. In this paper discusses the performance of single phase seven level Z (impedance) source cascaded H-bridge inverter topology suited for solar photovoltaic systems. A modified sinusoidal pulse width modulation technique is used to control the switches of the H-bridge inverter. The simulation results are obtained interms of inverter output voltage and harmonic analysis confirm improvement in voltage boost and reduction in harmonic distortion of the suggested inverter topology. The experimental results matches with the simulation values, as verified through a scaled down prototype.

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1. INTRODUCTION

Distributed energy systems employing fuel cell and PV array can easily configure with different topologies of power conversion units for example multilevel inverters are implemented for electrification over the years. Recent advancements of multilevel inverters either in their operating principle and modulation strategy focused for industrial applications and utility systems are found to be interesting and growing for the applicatons of reactive power compensation, renewable energy system power conversion, resonance circuit, UPS power conversion unit and electric-drive vehicles [1-6].

Multi-level inverters are designed with photovoltaic voltage source, semiconductor switching device and capacitor, and their performance and output are evaluated by their step. The semiconductor switching device must be able to withstand the voltage surge that occurs when switching switches. The main function of multilevel inverters is to convert the dc power to the desired amount of ac power [7, 8]. The topic under study is cascaded multilevel inverter, which is modular in nature and it can be configured with multiple modules [9-13]. Non-transformer power converters are used for the purpose of making such a system low cost, which is the unique function of multilevel inverters are as described in [14-20]. Merits and demerits of cascaded multi-level inverters are discussed through many applications in [21-24]. Infusion of Z-source network into the existing multilevel and other inverter topologies improves the voltage boosting capability which can be preferably used for photovoltaic systems [25, 26]. In this paper, Z-source Cascaded H-bridge multi-level inverter with symmetric configuration its steady-state operation is discussed in section 2, the

employed modulation technique is explained in section 3, Simulation and its experimental discussions are dealt in subsequent sections.

2. TOPOLOGY DESCRIPTION: Z-SOURCE CASCADED MLI FOR PV SYSTEMS

Figure 1 shows the three H-bridges are connected in cascade mode to convert the photovoltaic array dc output to the desired ac power. The output of these three bridges is added together and calculated as the total added value of the inverter. The seven level stepped expression of this system is built in Figure 2.

Each photovoltaic panel is connected in series and parallel connection mode and their output is connected to each individual H-bridges. The voltage output of H-bridges depends on the value of the photovoltaic system input to them. Also the number of H-bridges depends on the number of photovoltaics array in that system. Better voltage and current can be obtained in sinusoidal design by increasing the levels of the inverter. Also multi-level is considered to be very effective when compared to two level converter. This allows the use of smaller low-pass filters for harmonic reduction [27, 28].

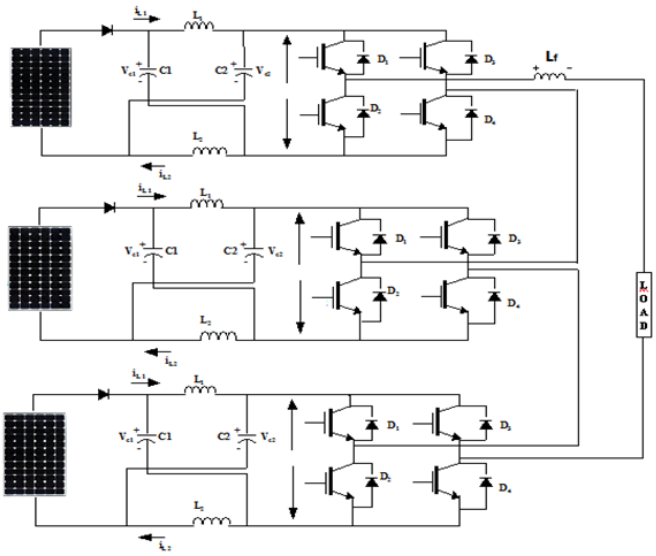

Figure 1. Power circuit of a single phase seven level Z-source cascaded H-bridge inverter

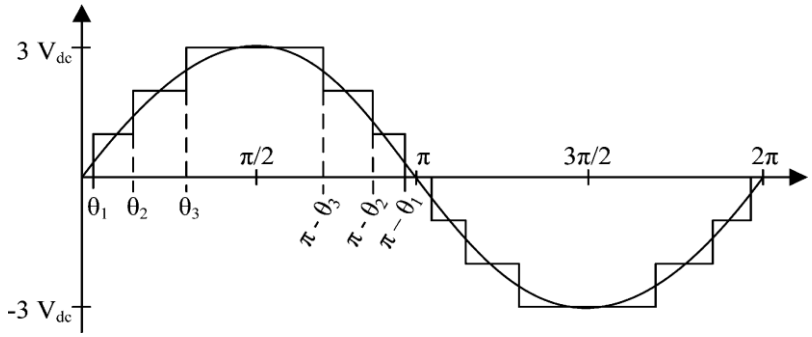

Figure 2. Output voltage waveform of single phase seven level Z-source cascaded H-bridge inverter

The proposed single phase seven level cascaded H-bridge Z-source inverter topology is formed by having photovoltaic array connected series interlinked single phase two level inverter and its output voltage is depends on the number of single phase inverter connected in circuit. The number of output voltage levels (m) in the phase voltage of symmetrical cascaded MLI is given by

$$q = 2N + 1 \quad (1)$$

Where, N-number of single phase inverter. In other words, a typical cascade MLI requires a photovoltaic arrays for $2N + 1\ level$.

If the inverter phase voltage steps is calculated as a value of q, then the line voltage of the inverter is calculated as

$$k = 2q + 1 \tag{2}$$

and also the steps level for three phase different types of load connection can be calculted as

$$p = 2k - 1 \tag{3}$$

The ac output voltage of the each single phase H-bridge inverter and the total sum of output voltage (V_o) value of the multilevel inverter as determined by using (4).

$$V_o = V_{dc1} + V_{dc2} + V_{dc3} \tag{4}$$

The cascaded H-bridge multi-level inverter desired sinusoidal output voltage can calculate by using using (5).

$$V_o = V_m \sin(\omega t) \tag{5}$$

To design cascaded multilevel inverter required number of switches for each phase or each H-bridge can estimate as per (6).

$$N_{sw} = 4N \tag{6}$$

The operating principle of ZSI Module can be explained as follows. The Z-source inverter is operating at two state of operation such as shoot-through and non-shoot-through states. When the inverter is operating at shoot-through state, the photovoitaic dc output power is coverting into ac power and non-shoot-through states condition the power conversion is zero because of dc-link voltage is zero.

The power balance equation of the each Z-source inverter as

$$\nu_{PN} \text{ x } i_{PN} \text{ x } (1-D) + 0 \text{ x } D = \nu_a \text{ x } i_a \tag{7}$$

Where, ν_{PN} and i_{PN} are each H-bridge inverter input voltage and current values, V_a and i_a are the each H-bridge inverter output voltage and current values and D is a duty ratio of the Z-source inverter.

The Z-source inverter output voltage is determined as

$$\nu_a = m \text{ x } \nu_{PN} \tag{8}$$

Where m defined as M sin ωt, M - modulation index.

From (7) and (8), i_{PN} is deduced as

$$i_{PN} = \frac{MIa}{2(1-D)}(cos\,\phi - cos(2\omega t - \phi)) = I_{PN} + \tilde{\imath}_{PN} \tag{9}$$

Both I_{PN} and $\tilde{\imath}_{PN}$affect the module variables i_{L1}, i_{L2}, v_{C1} and v_{C2}.

$$\begin{aligned} i_{L1} &= I_{L1} + \tilde{\imath}_{L1} i_{L2} = I_{L2} + \tilde{\imath}_{L2} \\ v_{C1} &= V_{C1} + \tilde{v}_{C1} v_{C2} = V_{C2} + \tilde{v}_{C2} \end{aligned} \tag{10}$$

The impedance design of ZSI network [29] is given by

$$L = \frac{2V_{PV}DT_s(1-D)}{3K_i MI_m \cos\phi} \quad \& \quad C = \frac{3DT_s MI_m \cos\phi}{8K_v V_{PV}(1-D)} \tag{11}$$

T_s, I_m and ϕ are the Switcing time period, maximum phae current and angle between the voltage and current on inverter output. K_v and K_i are voltage and current ripple factors.

3. MODULATION TECHNIQUE

Phase shifted sinusoidal PWM switching strategy can be widely adopted for cascaded ZSI which is based on classical sinusoidal pulse width modulation. Here the triangular signal is taken as the carrier and the signal is compared to the sinusoidal modulating signal. The frequency value of the output voltage of the inverter depends on these two signals. The output frequency value of the inverter can be changed to the desired level by changing the signal frequency of the triangular carrier. The triangular carrier signal frequency is taken as an odd multiplier for the elimination of even harmonics at the output of the inverter.

The triangular carrier signal is (N_c) responsible for the switching losses of the each inverter. So by selecting the right triangular carrier it is possible to get effective inverter output voltage with low conversion losses.

The number of carriers, n_c essential to generate m-level inverter output is given by

$$n_c = m - 1 \tag{12}$$

All the triangular carrier signals have the same peak-peak amplitude and frequency which are designated as A_c and f_c respectively, whereas the single sinusoidal reference or modulating signal has peak-peak amplitude of A_m and carrier frequency f_m. Sinusoidal signal as considered as a reference signal is always matched with the carrier sigan of triangular signal. When the sinusoidal signal amplitude is more than the triangular signal amplitude, the swithching pulse is produced and it's given to the inverter gate signal.

The important factors of the modulation procedure [30-36] are the ratio of the carrier and reference frequency $k=f_c/f_m$, where, f_c and f_m are frequency of the triangular and the sinusoidal signal, respectively. The modulation index $M = A_m / (m' * A_c)$, $m'= (m-1)/2$. Where A_m, A_c and m are the modulating signal amplituted, peak-peak triangular signal amplitude and inverter output level, respectively. Traditionally, the output voltage of the inverter can be express in Fourier series expansion as

$$V_{pn}(\omega t) = \sum_{n=1}^{\infty} V_n(a_n cosn\omega t + b_n sinn\omega t) \tag{13}$$

When the value is $a_0 = a_n = 0$, the inverter is operating at odd symmetric condition, it is represented in (14) Fourier series form.

$$V_{pn}(\omega t) = \sum_{n=1}^{\infty} V_n \sin(n\omega t) \tag{14}$$

4. SIMULATIONS AND DISCUSSIONS

Table 1 shows the simulation parameters used for the proposed inverter, having DC voltage sources, Z network parameters and a resistive load. Simulations have been developed in MATLAB/SIMULINK environment.

The output voltage of the each H-bridge inverter is obtained by employing the gate pulse. The output voltage of the each H-bridge inverter delivers in the shape of alternating quasi-square waveform. Figure 3 shows the switching timings of the inverter to produce a quasi-square output waveform by phase shifted pulse width modulation method for A=5 and f=50.

Various simulated waveforms like boosted DC link voltages, voltage across the three H-bridges, and output AC voltages (Voltage waveform across the three bridges and the load) are shown in Figure 4 and Figure 5.The rms voltage obtained for the proposed inverter is 32.73 V with Z network and 28.88 V without Z network. Adding Z network boosts the voltage by 13.33%. The obtained peak voltage is about 45.27 V with a THD value of 21.20%. Also, the peak voltage across the the three H-bridges are 14 V, 15.27 V and 16.01 V with THD values of 32.21%, 31.17% and 41.44% respectively. However, adding suitable value of inductorfilter will subsequently reduce the THD within 5% with the same peak voltage.

Figure 6 is showing simulated output ac voltage observed through Fourier window and Figure 7 is showing filtered (Using inductor filter, Lf) phase voltage waveform

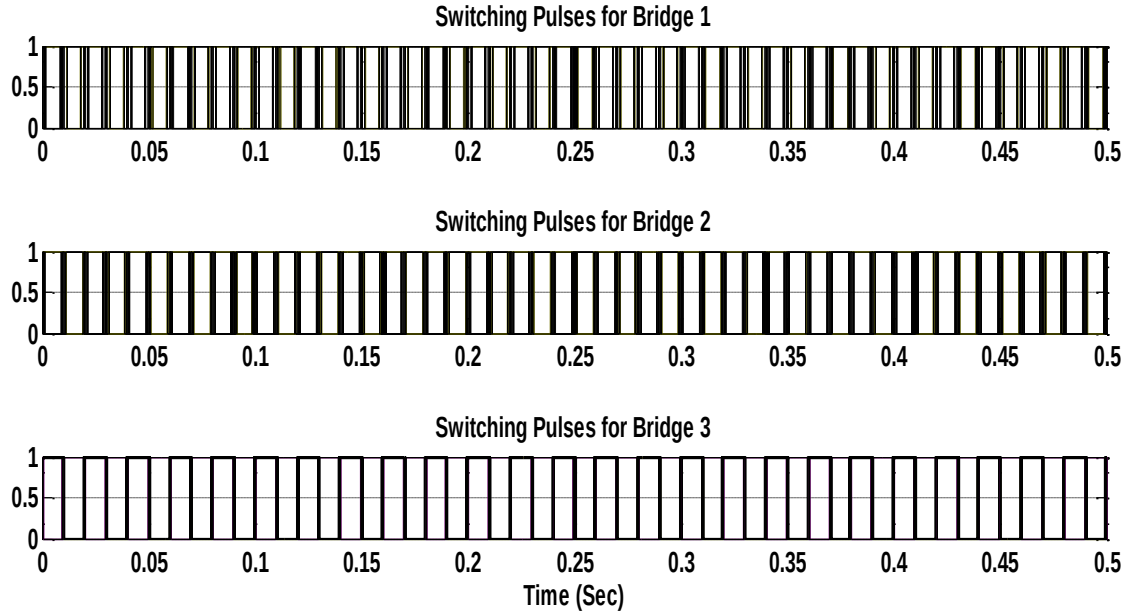

Figure 3. Switching pulses generation for the bridges 1, 2 and 3

Table 1. Simulation parameters

Components	Parameters
DC voltage sources (V_{dc1} , V_{dc2} V_{dc3})	12 V each
Z network	
$L_1 – L_6$	40 mH
$C_1 – C_6$	6000 µF
Inductor filter (L_f)	40 mH
Resistive Load (R)	50 Ω

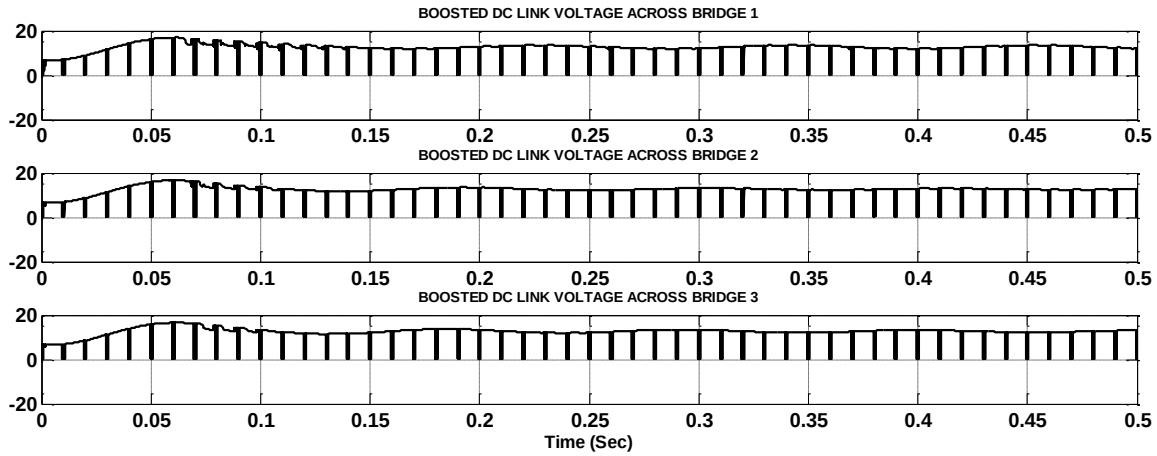

Figure 4. Boosted DC link voltages, appeared across the bridges 1, 2 and 3 (top to bottom)

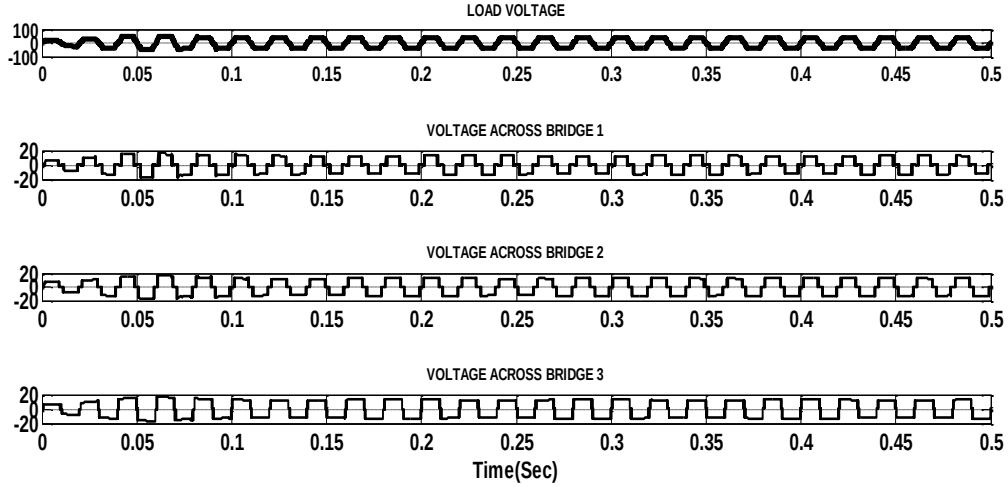

Figure 5. Simulated output AC voltages (voltage waveform across bridges 1, 2, 3 and the load) (top to bottom)

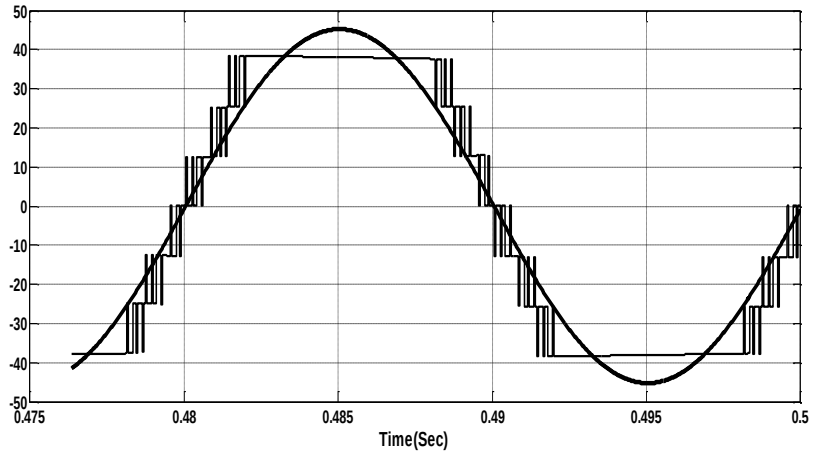

Figure 6. Simulated output ac voltage observed through Fourier window

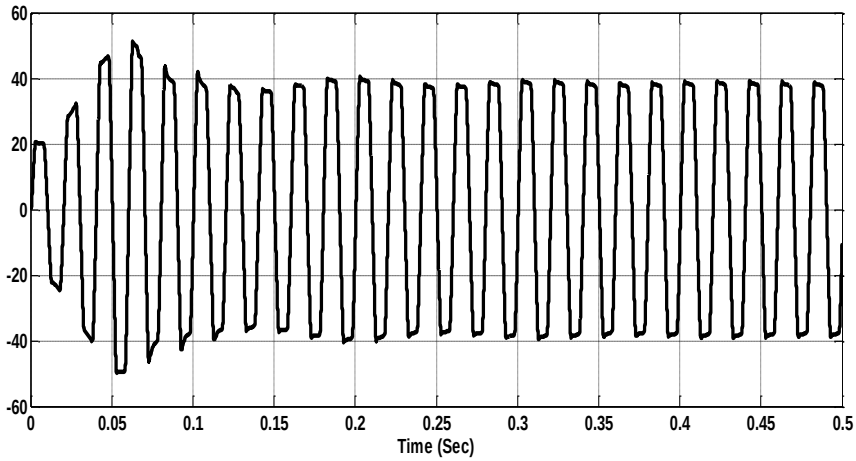

Figure 7. Filtered (Using inductor filter, Lf) phase voltage waveform

5. EXPERIMENTAL RESULTS

The proposed seven-level cascaded Z-source inverter circuit has been tested with three DC sources of 12 V with an R load of 50 Ω and the other test parameters used for simulation. The control scheme is programmed with a fixed-point TI-TMS3202812 digital signal processor (DSP) and a programmable logic device. The control signals are sent to insulated gate bipolar transistors (IGBTs) through optical fiber cables. The phase-shifted pulse width modulation technique has been implemented for controlling a seven-level cascaded Z source inverter feeding a resistive load. The sectionalized view of various components present in the overall experimental setup is shown in Figure 8. It consists of a power supply section, provided to give dc supply to the driver circuit and inverter section for energizing the various passive elements present in it. The regulated dc supply of +5 V and ± 15 V is given to the driver circuit IR 2110 and inverter section respectively through IC's LM 7805, LM 7815 and LM 7915 after buffering actions with low noise immunity with respect to output impedance variations. The switching signals to these IGBT switches are given through IR 2110 drivers with autonomous high and low side referenced output channels which operate up to 500 volts with a feature of high pulse current buffer stage designed for minimum driver cross conduction of standard CMOS output, down to 3.3 V logic suitable for inverter applications.

Optoisolator IC TLP 250 is used for gate driving purposes and IC 4506, IC 4081 for buffering actions. Control signals obtained from the FPGA controller are given to the inverter section through these IC's. The inverter circuit module uses IGBT pack namely FSBB20CH60F IC with protection and gate driving functions.XILINX Spartan 3E FPGA XC3S100E, Field programmable gate array (FPGA) has been chosen to implement the pulse width modulation due to its fast prototyping, simple hardware, and software design. DC voltage of 12V is given to the three H-bridges individually and the output voltage waveform is observed through a power analyzer generating output magnitude of 38 V with grid frequency nearly 50 Hz which is shown in Figure 9. FFT spectrum of the output voltage waveform is measured showing a THD value of 9.4% as shown in Figure 10.

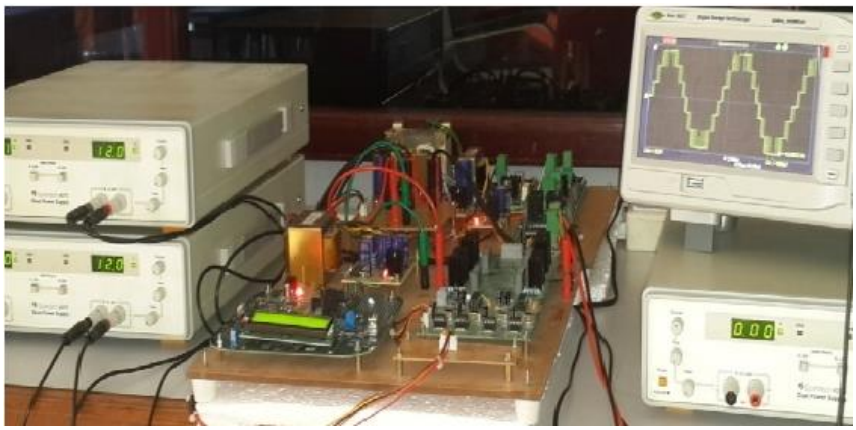

Figure 8. Experimental setup of the system

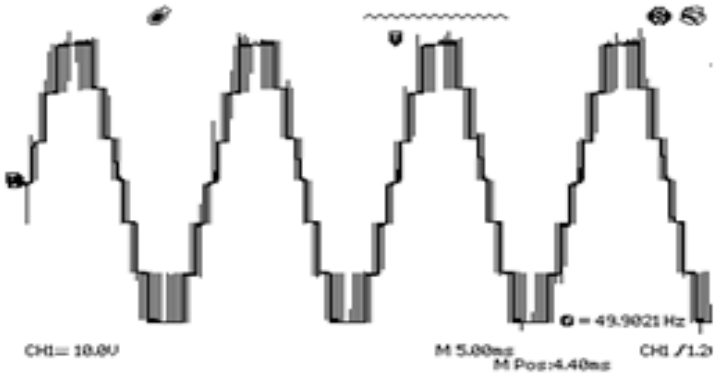

Figure 9. Experimental voltage waveform measured across the resistive load

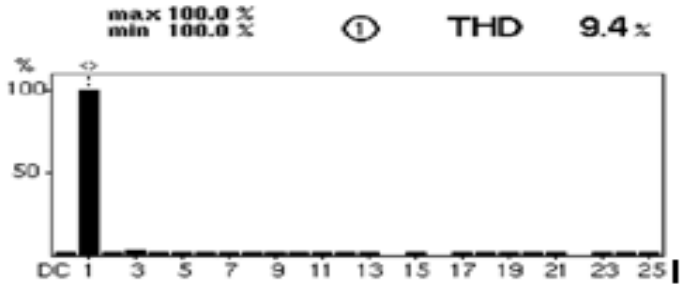

Figure 10. FFT spectrum of the experimental voltage waveform

6. CONCLUSION

Z-source cascaded multilevel inverters play an important role in various power conversion places. They are off-grid and grid integrated solar photovoltaic system, fuel cell, UPS power conversion systems. This multilevel inverter has low electromagnetic interference, high operating efficiency, low switching loss, high quality voltage and higher operating voltage. The simulation and hardware results reach a decision to a excessive level. The proposed inverter exhibits well performance and is most suitable for solar photvoltaic applications.

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